REMARKS

35 USC Section 102 Rejections

The above referenced Office Action rejects independent Claims 1-3, and 7-23 as being anticipated by Yaŋg (US 6,553,472). Applicants respectfully traverse.

In the "response to argument" section of the above referenced Office Action, it is stated that the cited Yang reference discloses programmer input and that the memory controller of Yang calibrates and adjusts intra-cycle timing relationships based upon the programmer input. It is further stated that the device of the Yang reference requires the initial programming input and based upon that input, calibrates and adjust timing of the device. Applicants respond by reiterating that a process requiring user input, or a process requiring a programmer to set initial parameters of multiple signals for the device is not automatically calibrating as in the claimed invention. Accordingly, to further distinguish over the teaching of the Yang reference, Applicant have amended independent Claims 1, 7, and 12 to specifically recite the automatic adjusting of the claimed invention is free of user input.

Accordingly, Claim 1 has been amended to recite a method for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device.

The method includes generating command signals for accessing an integrated circuit component, accessing data signals for conveying data for the integrated circuit component, accessing sampling signals for controlling the sampling of the data signals, and automatically adjusting a phase relationship between the command signals, the data signals, and the sampling signals to calibrate operation of the integrated circuit device. Applicant points out that the claimed embodiments recite automatic calibration of the cycle timing relationships. Applicants further point out that the automatic adjusting is free of user input. The automatic calibration can be performed by, for example, the memory controller.

In contrast, the Yang reference would not be operable without the programming of its inputs. Yang discloses a method for programming clock delays, command delays, read command parameter delays, and write command parameter delays of a memory controller. Yang does not disclose the automatic calibration and the automatic adjusting as in the claimed embodiments of the present invention. For example, at col. 4 at line 25-34, Yang states that the "...programmable parameters for the MC required for correct and optimum I/O operation with the MC and SDRAM need to be specified. Table 2 lists and describes seventeen related programmable parameters in the MC. Other programmable parameters, such as refresh control and SDRAM initialization parameters are not listed. These timing

parameters are necessary for I/O operations such as memory read, memory write, same bank access, different bank access, etc."

Automatic calibrating and automatic adjusting limitations are included in each of the independent claims of the present application. Applicant asserts that Yang describes programming memory controller to operate at the desired point. This is different from automatically calibrating and automatically adjusting, which does not require any programmer input. Furthermore, independent Claims 1, 7 and 12 have also been amended to especially recite that the automatic adjusting is free of user input.

With respect to Claim 12, independent Claim 12 recites a method for finding an operating mode for a DRAM component by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DRAM component, by automatically altering a phase relationship between the command signals, the data signals, and the sampling signals to determine an operating mode of the DRAM component, without requiring a valid initial operating point to exist within the specified operating parameters for the DRAM component. There is no teaching or suggestion of any situation within Yang for dealing with a case where the DRAM component is not operable within the specified parameters. As pointed out in the response to argument of the above referenced Office Action,

the Yang reference requires operation within the specified parameters that are input by the user/programmer. Yang would not know how to operate with and "out of spec" DRAM component.

Accordingly, Yang does not show or suggest the claimed invention as recited in independent Claims 1-22 and therefore Claims 1-22 are not anticipated by Yang within the meaning of 35 USC Section 102.

35 USC Section 103 Rejections

The above referenced Office Action rejects Claims 4-6, 9-11, 13-22, and as being rendered obvious by Yang in view of Suzuki (US 2004/0160833), Keeth (US 6016282) and Davis (US 5781766). Applicants respectfully traverse.

As described above, Applicant asserts that Yang does not disclose the automatic calibration and the automatic adjusting as in the claimed embodiments of the present invention. The addition of Suzuki does not cure this defect. Suzuki is relied upon for showing a memory controller that controls DDR SDRAM. As with Yang, Suzuki does not show or suggest the automatic calibration and automatic adjusting as in the claimed embodiments of the present invention.

Accordingly, Applicants assert that the claimed invention as recited in Claims 1-22 is not shown or suggested by the combination of Yang and Suzuki, and therefore, Claims 1-22 are not rendered obvious by the Yang and Suzuki combination within the meaning of 35 USC Section 103.

With respect to dependent Claims 13 and 19, additional limitations are added that recite performing a coarse calibration by altering the phase relationship in accordance with a large step interval to find the operating mode of the DRAM component, and performing a fine calibration by altering the phase relationship in accordance with a small step interval to optimize the operating mode of the DRAM component. The cited section of the Keeth reference (e.g., Keeth col. 4 lines 11-18 and col. 7 lines 44-51) describes the adjustment of a variety of vernier circuits within each DRAM to implement the timing adjustment. There is no description of any coarse versus fine calibration. Additionally, the vernier circuits are adjusted within the DRAMs, not the memory controller as in the claimed invention. Applicant point out that this is in addition to the fact that the DRAM component may not have a valid initial operating point within the specified operating parameters. The cited references do not mention scenarios for handling functionally dead or "out of spec" DRAM components.

With respect to dependent Claims 14 and 20, further limitations are added describing the configuring of the memory controller to operate with the DRAM component in accordance with an optimal operating mode, wherein the optimal operating mode is determined via the fine calibration. As described above, there is no description of any coarse versus fine calibration in the cited references. The added limitations further describing the fine calibration further distinguish over the cited references.

With respect to Claim 18, Claim 18 recites a computer readable media for finding an operating mode for a DDR DRAM component by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DDR DRAM component, and automatically altering a phase relationship between the command signals, the DQ signals, and the DQS signals to determine an operating mode of the DDR DRAM component, without requiring a valid initial operating point within the specified operating parameters for the DRAM component. There is no teaching or suggestion of any situation within Yang or Suzuki for dealing with a case where the DRAM component is not operable within the specified parameters. As pointed out in the response to argument of the above referenced Office Action, the Yang reference requires operation within the specified parameters that are input by the user/programmer. Yang would not know how to operate with and "out of spec" DRAM component.

Respect to independent Claim 22, Claim 22 recites a method performed by a memory controller comprising automatically altering a phase relationship between the command signals, the data signals, and the sampling signals transmitted via a PCB to determine an operating mode of the DRAM component, wherein the DRAM component is inoperable at specified operating parameters, and wherein said automatic altering is performed free of user input. For the rationale described above, Yang and Davis do not show automatic calibration free of user input. Additionally, with respect to the Davis reference, the cited section of Davis (e.g., col. 2 lines 30-40) does not show any automatic establishment of an operating mode when the DRAM component is inoperable within its operating parameters.

CONCLUSION

The Examiner is urged to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application. Please charge any additional fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,
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Dated: 10/29, 2007

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